VOLTAGE BOOSTER

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to integrated circuit devices and, in particular, to voltage boosters and pass circuits for the decoding and passing of programming voltages in memory devices.

BACKGROUND OF THE INVENTION

[0002] Memory devices are typically provided as internal storage areas in the computer. The term memory identifies data storage that comes in the form of integrated circuit chips. In general, memory devices contain an array of memory cells for storing data, and row and column decoder circuits coupled to the array of memory cells for accessing the array of memory cells in response to an external address.

[0003] One type of memory is a non-volatile memory known as Flash memory. A flash memory is a type of floating-gate memory device that can be erased and reprogrammed. Many modern personal computers (PCs) have their BIOS stored on a flash memory chip so that it can easily be updated if necessary. Such a BIOS is sometimes called a flash BIOS. Flash memory is also popular in wireless electronic devices because it enables the manufacturer to support new communication protocols as they become standardized and to provide the ability to remotely upgrade the device for enhanced features.

[0004] A typical flash memory comprises a memory array that includes a large number of memory cells arranged in row and column fashion. Each of the memory cells includes a floating gate field-effect transistor capable of holding a charge. The cells are usually grouped into blocks. Each of the cells within a block can be electrically programmed by charging the floating gate. The charge can be removed from the floating gate by a block erase operation. The data in a cell is determined by the presence or absence of the charge in the floating gate.

[0005] Flash memory typically utilizes one of two basic architectures known as NOR flash and NAND flash. The designation is derived from the logic used to read the devices. In NOR flash architecture, a column of memory cells are coupled in parallel with each memory

cell coupled to a bit line. In NAND flash architecture, a column of memory cells are coupled in series with only the first memory cell of the column coupled to a bit line.

[0006] An advantage of NAND flash architecture is that it facilitates a smaller array size due in part to a smaller word line pitch. However, programming voltages of NAND flash architecture are generally higher than those of NOR flash architecture.

[0007] Because the programming voltages of NAND flash architecture are generally several times the supply potential, it becomes difficult to pass these high-voltage control signals through the circuit without loss. In general, an n-channel field-effect transistor (nFET) with a positive Vt requires a gate voltage higher than the voltage being applied to its drain in order to pass the drain voltage to the source.

[0008] Voltages higher than the supply potential are typically generated internally to a memory device using a charge pump or other voltage generator. Because a voltage generator is required for each voltage concurrently utilized by the device, it is preferable to minimize the number of voltage levels required by the device.

[0009] Memory devices generally include some type of boost circuit to provide sufficient gate voltage to an nFET passing the high programming voltage. While the gate voltage must generally be above the programming voltage by a value equal to the threshold voltage, Vt, of the nFET, higher gate voltages will permit correct operating voltages and improved programming speed.

[0010] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for alternate methods and circuits for passing high-voltage control signals in an integrated circuit device.

SUMMARY OF THE INVENTION

[0011] The above-mentioned problems with memory devices and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0012] The various embodiments of the invention include voltage boosters or pass circuits for generating a boosted voltage. The boosted voltage can be used as a gate voltage for a pass gate providing programming voltages to a selected block of memory cells, such as in a NAND flash memory array. The pass circuits facilitate the elimination of high-voltage p-channel devices by providing a boosted voltage using n-channel devices. Decoder circuits utilizing such pass circuits are expected to be smaller in size due to the elimination of an N-well from the decoder area. The pass circuits further permit control of multiple pass gates using a single boosted voltage source.

[0013] The invention provides methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] Figure 1 is a functional block diagram of a basic flash memory device in accordance with an embodiment of the invention coupled to a processor.

[0015] Figure 2 is a schematic of a portion of a block of a memory array in accordance with an embodiment of the invention.

[0016] Figure 3A is a schematic of a voltage booster or pass circuit in accordance with one embodiment of the invention.

[0017] Figure 3B is a schematic of a voltage booster or pass circuit in accordance with an further embodiment of the invention.

DETAILED DESCRIPTION OF THE INVENTION

[0018] In the following detailed description of the present embodiments, reference is made to the accompanying drawings that form a part hereof, and in which is shown by way of illustration specific embodiments in which the inventions may be practiced. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention, and it is to be understood that other embodiments may be utilized and that process, electrical or mechanical changes may be made without departing from the scope of the present invention. The terms wafer and substrate used in the following description include any

base semiconductor structure. Both are to be understood as including silicon-on-sapphire (SOS) technology, silicon-on-insulator (SOI) technology, thin film transistor (TFT) technology, doped and undoped semiconductors, epitaxial layers of a silicon supported by a base semiconductor structure, as well as other semiconductor structures well known to one skilled in the art. Furthermore, when reference is made to a wafer or substrate in the following description, previous process steps may have been utilized to form regions/junctions in the base semiconductor structure, and terms wafer or substrate include the underlying layers containing such regions/junctions. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[0019] Figure 1 is a functional block diagram of a basic flash memory device 101 that is coupled to a processor 103. The memory device 101 and the processor 103 may form part of an electronic system 100. The memory device 101 has been simplified to focus on features of the memory that are helpful in understanding the present invention. The memory device 101 includes an array of non-volatile memory cells 105. The memory array 105 may utilize an NAND flash architecture.

[0020] Each memory cell is thus located at an intersection of a word line and a local bit line. The memory array 105 is arranged in rows and columns, with the rows arranged in blocks. A memory block is some discrete portion of the memory array 105. Individual word lines generally extend to only one memory block while bit lines may extend to multiple memory blocks. The memory cells generally can be erased in blocks. Data, however, may be stored in the memory array 105 separate from the block structure.

[0021] A row and block decoder 109 and a column decoder 111 are provided to decode address signals provided on address lines A0-Ax 113. The row and block decoder 109 includes at least one pass gate in accordance with an embodiment of the invention. An address buffer circuit 115 is provided to latch the address signals. Address signals are received and decoded to access the memory array 105. Sense and latch circuitry 119 act as sense amplifiers during read and data input program operations. The number of the latches in the sense and latch circuitry is usually the same as the number of bits per page of the memory array 105. Cache latches 120 interface to the I/O through the column decoder multiplexers

121. Data is loaded into the cache latches 120, or read from the cache latches 120, through the column decoder multiplexers 121. The cache latches 120 provide pipelining by permitting data loaded into the sense and latch circuitry 119 to be written to the memory array 105 while concurrently loading new data into the cache latches 120, thereby improving the programming data rate. The column decoder multiplexers 121 select one or more columns of the data from the cache latches 120 in response to control signals from the column decoder 111.Input buffer circuit 123 and output buffer circuit 125 are included for bi-directional data communication over a plurality of data (DQ) lines 127 with the processor 103.

[0022] Command control circuit 131 decodes signals provided on control lines 135 from the processor 103. These signals are used to control the operations on the memory array 105, including data read, data write, and erase operations. Input/output control circuit 133 is used to control the input buffer circuit 123 and the output buffer circuit 125 in response to some of the control signals. As stated above, the flash memory device 101 has been simplified to facilitate a basic understanding of the features of the memory. A more detailed understanding of flash memories is known to those skilled in the art. As is well known, such memory devices 101 may be fabricated as integrated circuits on a semiconductor substrate.

[0023] Figure 2 is a schematic of a portion of a block of the memory array. The memory array contains floating-gate memory cells 206 coupled in a NAND configuration, i.e., memory cells 206 coupled in series strings, with a first memory cell 206 selectively coupled to a bit line 204 through a string select transistor, such as nFET 218. The nFETs 218 are responsive to a control signal received on node 208. Similarly, the last memory cell 206 is selectively coupled to a node 222 through a ground select transistor, such as nFET 220. The nFETs 220 are responsive to a control signal received on node 210.

[0024] The word lines 202 receive programming voltages in response to the row decoder 212. Typically, in programming a NAND flash memory device, a selected word line 202 will receive a programming voltage, Vpp, while unselected word lines 202 will receive an intermediate voltage, Vm, between the supply voltage Vcc and the programming voltage Vpp. As an example, the programming voltage Vpp may be approximately 15V-20V while the intermediate voltage Vm may be approximately 10V.

[0025] The word lines 202 are selectively coupled to the memory cells 206 through pass gates, such as nFETs 216. To efficiently pass the programming voltages Vpp from the word lines 202 to the gates of the selected row of memory cells 206, the pass gates 216 are provided with a boosted gate voltage Vpp+ from the block decoder 214. The boosted gate voltage Vpp+ is preferably at least one threshold voltage Vt of the pass gates 216 above the programming voltage Vpp.

[0026] The boosted gate voltage Vpp+ is generated by a pass circuit that can be considered as part of the block decoder 214, although it may be responsive to the block decoder 214 without being part of the decoder itself. Figure 3A is a schematic of a voltage booster or pass circuit 300A in accordance with one embodiment of the invention.

[0027] The pass circuit 300A includes an input node 306 for receiving the programming voltage Vpp and an output node 336 for providing a boosted voltage Vpp+. It should be noted that while the discussion is in the context of the programming voltage Vpp for a flash memory device, the pass circuit 300A may be used to provide a voltage at its output node 336 that is boosted from a voltage at its input node 306, regardless of the application. For one embodiment, the output node 336 represents the output of the block decoder 214 of Figure 2.

[0028] The pass circuit 300A further includes a first capacitor 320 coupled to receive a CLK* signal at a first terminal and a second capacitor 322 coupled to receive a CLK signal that is the complement of the CLK* signal at its first terminal. While these clock signals may be coupled directly to the capacitors 320 and 322, the pass circuit 300A is depicted to include circuitry for selectively activating or deactivating the pass circuit 300A.

[0029] In the embodiment depicted in Figure 3A, selective activation is facilitated by providing a block select signal to the node 304 as a first input to the NAND gate 312. The block select signal may be buffered, such as passing it through the series-connected inverters 308 and 310. The second input of the NAND gate 312 is coupled to node 302 to receive a clock signal CLK. By setting the block select signal to a logic high value, e.g., the supply voltage Vcc, the output of the NAND gate 312 is responsive to the clock signal on node 302, thus activating the pass circuit 300A. By setting the block select signal to a logic low value, e.g., the ground potential Vss, the output of the NAND gate 312 is forced to a logic high, thus deactivating the pass circuit 300A. While the various embodiments are described using a

clock signal having an amplitude equal to Vcc, other amplitudes could also be used. Additionally, it is noted that other combinatorial logic could be utilized in place of the logic gates of the pass circuit 300A to apply the appropriate voltages for proper operation of the boost circuitry as described herein.

[0030] When activated, the output of the NAND gate 312, having the clock signal CLK applied to its second output, is the complementary clock signal CLK*. The clock signal CLK* may be buffered, such as passing it through the series-connected inverters 314 and 316. The output of the inverter 316 is then provided to the capacitor 320 as the clock signal CLK*. The clock signal CLK* at the output of the inverter 316 is then inverted by the inverter 318 and provided to the capacitor 322 as the clock signal CLK.

[0031] A first n-channel field-effect transistor (nFET) 324 has a gate coupled to a second terminal of the capacitor 320, a first source/drain region coupled to the node 306 and a second source/drain region coupled to the gate of the second nFET 326. The second nFET 326 has a first source/drain region coupled to the first source/drain region of the first nFET 324 and a second source/drain region coupled to the gate of a third nFET 328. The third nFET 328 has a first source/drain region coupled to its gate and a second source/drain region coupled to the output node 336.

[0032] A fourth nFET 330 has its gate coupled to a node 334, a first source/drain region coupled to a second terminal of the second capacitor 322 and a second source/drain region coupled to receive the block select signal or other activation signal. A fifth nFET 332 has its gate coupled to the node 334, a first source/drain region coupled to the gate of the third nFET 328 and a second source/drain region coupled to receive the block select signal or other activation signal. Node 334 is coupled to receive a supply voltage, such as Vcc.

[0033] Upon activation at node 304, the gates of the nFETs 324, 326 and 328 will be brought up to a voltage substantially equal to the voltage level of the block select signal minus the threshold voltages of the associated nFETs 330 and 332, i.e., Vcc – Vt. The nFETs 324, 326 and 328 will thus be activated, allowing at least the voltage of node 306, i.e., Vpp, to pass to node 336. As the clock signals CLK and CLK* cycle, capacitive coupling will pull up the potential levels to the gates of the nFETs 324, 326 and 328.

[0034] The potential level to the gate of the nFET 328 will reach a maximum value approximately equal to:

$Vpp + Vcc * k_1$;

where $k_1 \approx C_{320} / (C_{320} + C_{324} + C_{328} + Cj_{328} + C_{out})$

C_{320} = capacitance of the capacitor 320

C_{324} = gate capacitance of the nFET 324

C_{328} = gate capacitance of the nFET 328

Cj_{328} = junction capacitance of nFET 328

C_{out} = output capacitance at node 336

It is noted, however, that Cj_{328} can generally be assumed to have an insignificant impact on the value of k_1.

[0035] The potential level to the gate of the nFET 326 will reach a maximum value approximately equal to:

$Vpp + Vcc * k_2$;

where $k_2 \approx C_{322} / (C_{322} + C_{326} + Cj_{324} + Cj_{330})$

C_{322} = capacitance of the capacitor 322

C_{326} = gate capacitance of the nFET 326

Cj_{324} = junction capacitance of the nFET 324

Cj_{330} = junction capacitance of the nFET 330

It is noted, however, that Cj_{324} and Cj_{330} can generally be assumed to have an insignificant impact on the value of k_2.

[0036] To pass the potential from the input node 306 to the output node 336, $Vcc * k_1$ must be at least equal to the Vt of the third nFET 328 and $Vcc * k_2$ must be at least equal to the Vt of the second nFET 326. These constraints determine the minimum sizing of the capacitors 320 and 322. However, to generate a boosted voltage at the output node 336, the

capacitors 320 and 322 should be sized such that Vcc * k_1 is greater than the Vt of the third nFET 328 and Vcc * k_2 is greater than the Vt of the second nFET 326. It is more preferable that the capacitor 320 be sized such that Vcc * k_1 >= Vt of nFET 328 + Vt of the pass gate it is expected to control, thereby permitting the pass gate to fully pass Vpp.

[0037] Improvements in efficiency of the boost circuitry can be realized by utilizing low-Vt transistors in the pass circuit. This can be accomplished by replacing the nFETs 324 and 326 of the pass circuit 300A with series-connected low-Vt transistors. Low-Vt transistors can have threshold voltages in the range of 0.2V to 0.3V. Therefore, the same potential can be passed to the output node while applying lower boosted voltages to the gates of the transistors. The efficiency of the boost circuitry is thus improved as it can operate at lower internal gate voltages of, e.g., nFETs 324a, 324b, 326a, 326b and 328. Figure 3B is a schematic of a pass circuit 300B in accordance with an embodiment of the invention facilitating the use of low-Vt transistors. It is noted that the use of series-connected transistors in the pass circuit 300B can also result in reduced current leakage during deactivation of the pass circuit.

[0038] Many of the components of pass circuit 300B are described with reference to the pass circuit 300A and will not be repeated here. Activation of the pass circuit 300B in response to a block select signal at node 304 occurs as described with reference to pass circuit 300A. In place of nFET 324, a pair of series-connected nFETs 324a and 324b are used. The pair of series-connected nFETs 324a and 324b has their common source/drain region selectively coupled to a potential node 350, such as through nFETs 342 and 344 or other selective coupling device. The nFET 342 is coupled to receive a control signal from node 338 to control is activation. The nFET 344 is coupled to receive a control signal from node 340 to control its activation.

[0039] In place of nFET 326, a pair of series-connected nFETs 326a and 326b are used. The pair of series-connected nFETs 326a and 326b has their common source/drain region selectively coupled to the potential node 350, such as through nFETs 346 and 348 or other selective coupling device. The nFET 346 is coupled to receive a control signal from node 338 to control is activation. The nFET 348 is coupled to receive a control signal from node 340 to control its activation. The potential node 350 is coupled to receive the supply voltage Vcc.

[0040] During deactivation of the pass circuit 300B, the gates of the nFET pair 324a/324b will be pulled to the ground potential Vss through the nFET 332. By coupling the shared source/drain regions of the nFET pair 324a/324b to the supply voltage Vcc, the gate-source voltage V_{GS} for the nFET 324a will be negative, thus reducing current leakage from node 306. The V_{GS} of the nFET 324b will be higher than that of the nFET 324a at approximately zero volts. However, it will still be deactivated and any current leakage through this nFET will generally be from the supply voltage at node 350 as opposed to the Vpp source at node 306.

[0041] Similarly, during deactivation of the pass circuit 300B, the gates of the nFET pair 326a/326b will be pulled to the ground potential Vss through the nFET 330. By coupling the shared source/drain regions of the nFET pair 326a/326b to the supply voltage Vcc, the gate-source voltage V_{GS} for the nFET 326a will be negative, thus reducing current leakage from node 306. The V_{GS} of the nFET 326b will be higher than that of the nFET 326a at approximately zero volts. However, it will still be deactivated and any current leakage through this nFET will generally be from the supply voltage at node 350 as opposed to the Vpp source at node 306.

[0042] For the pass circuit 300B, the potential level to the gate of the nFET 328 will reach a maximum value approximately equal to:

$$Vpp + Vcc * k_1;$$

where $k_1 \approx C_{320} / (C_{320} + C_{324a} + C_{324b} + C_{328} + Cj_{328} + C_{out})$

C_{320} = capacitance of the capacitor 320

C_{324a} = gate capacitance of the nFET 324a

C_{324b} = gate capacitance of the nFET 324b

C_{328} = gate capacitance of the nFET 328

Cj_{328} = junction capacitance of the nFET 324

C_{out} = output capacitance at node 336

It is noted, however, that Cj_{328} can generally be assumed to have an insignificant impact on the value of k_1.

[0043] For the pass circuit 300B, the potential level to the gates of the nFETs 326a and 326b will reach a maximum value approximately equal to:

$$Vpp + Vcc * k_2;$$

where $k_2 \approx C_{322} / (C_{322} + C_{326a} + C_{326b})$

C_{322} = capacitance of the capacitor 322

C_{326a} = gate capacitance of the nFET 326a

C_{326b} = gate capacitance of the nFET 326b

Cj_{324b} = junction capacitance of the nFET 324

Cj_{330} = junction capacitance of the nFET 330

It is noted, however, that Cj_{324b} and Cj_{330} can generally be assumed to have an insignificant impact on the value of k_2.

[0044] To pass the potential from the input node 306 to the output node 336, $Vcc * k_1$ must be at least equal to the Vt of the third nFET 328 and $Vcc * k_2$ must be at least equal to the Vt of the second nFETs 326a and 326b. These constraints determine the minimum sizing of the capacitors 320 and 322. However, to generate a boosted voltage at the output node 336, the first capacitor 320 and the second capacitor 322 should be sized such that $Vcc * k_1$ is greater than the Vt of the third nFET 328 and $Vcc * k_2$ is greater than the Vt of the second nFETs 326a and 326b. It is more preferable that the capacitor 320 be sized such that $Vcc * k_1$ >= Vt of nFET 328 + Vt of the pass gate it is expected to control, thereby permitting the pass gate to fully pass Vpp.

[0045] In operation, a programming command will be received by a memory device from a processor or other controller. The command will be accompanied by a location address identifying the memory cells to be programmed. After latching the address signals, the address will be decoded to identify the target block. The block decoder will generate the control signal indicative of a desire to access a block of memory cells. The control signal, i.e., the block select signal, will have a first logic level for selected blocks and a second logic level for unselected blocks. The pass circuits for selected blocks will be activated, thereby

generating the boosted voltage Vpp+ at their output for control of the pass gates on the word lines of the memory array. Rows of the selected blocks will then receive the voltage applied to their respective word lines, i.e., Vpp for selected word lines and a lower voltage for unselected word lines.

[0046] In the various embodiments of the invention, by providing a voltage boosted from Vpp, a single pass circuit can be used to activate pass gates for multiple rows of a selected block. This is advantageous over local pass circuits where each pass gate of each row of the block is provided with its own pass circuit. Using pass circuits of the type described herein, a single pass circuit can provide a gate voltage to a number of pass gates where that gate voltage has a potential level that exceeds Vpp by at least the Vt of the pass gate. This will permit a clean passing of the programming voltage to the memory cells without requiring individual pass circuits for each row.

CONCLUSION

[0047] Pass circuits for generating a voltage boosted from an input voltage are provided herein. Methods of operating these pass circuits, especially in relation to their use in controlling pass gates for NAND flash memory devices, are also provided herein. By providing a programming voltage as an input to the pass circuit and boosting it at least one Vt of the pass gates above the programming voltage, the resulting boosted voltage may be used to control multiple pass gates, e.g., each pass gate of a selected block of memory cells, while still permitting an unreduced programming voltage to be applied to the selected memory cells of the selected block of memory cells.

[0048] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.